AMENDMENTS TO THE SPECIFICATION

**Please replace paragraph [0007] with the following amended paragraph:**

**[0007]** One embodiment of the present invention can include a method of relieving timing-based congestion during physical implementation of an integrated circuit. The method can include routing a placed circuit design of the integrated circuit in a delay mode, wherein the routed circuit design includes at least one instance of connection sharing. An initial delay for connections of the circuit design can be calculated based upon the routing step. A final delay for connections of the circuit design can be predicted with [[were]] connection sharing ~~overlaps to be~~ removed. The final delays can be predicted according to the initial delays and a measure of connection sharing within the circuit design. Connections of the circuit design that do not conform with timing constraints based upon at least one of the initial delays or the [[and]] final delays can be identified. A detailed routing of the circuit design or further optimization of the identified connections of the circuit design can be performed based upon the identifying step.

**Please replace the Abstract with the following amended Abstract:**

A method of relieving timing-based congestion during physical implementation of a programmable logic device can include routing a placed circuit design for the programmable logic device in a delay mode and calculating an initial delay for connections of the circuit design based upon [[said]] the routing step. A final delay for connections of the circuit design can be predicted with [[were]] connection sharing ~~overlaps to be~~ removed. Connections of the circuit design that do not conform with timing constraints based upon at least one of the initial delays or the [[and]] final delays can be identified. Accordingly, a detailed routing of the circuit design or further optimization of the circuit design can be selectively performed according to the determination regarding the timing constraints.